

# Roughening, Etching, and Nanoscale Patterning of Silicon and Germanium

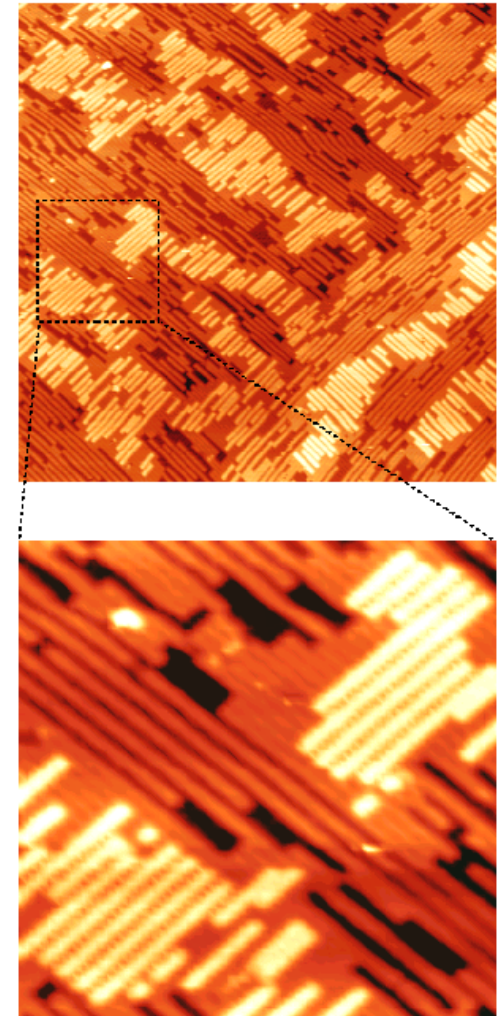
**John H. Weaver, University of Illinois, DMR-0301821**

Every one of the hundred-billion microelectronic chips made in the world each year undergoes many stages of material addition and material removal (etching) as complex 3D patterns are formed on the wafer. Exquisite control over such patterning comes from studies of surface reactions at the atomic level in real time at elevated temperature. Here, we show how Br roughens a silicon surface, a process that was completely unexpected and whose discovery forces a rethinking of semiconductor patterning.

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Scanning tunneling microscopy images of a Br-roughened Si surface. The narrow dark lines represent rows of missing atoms in the main layer and the bright features are rows of Si dimers.

24 h, 700 K, 100 X 100 nm<sup>2</sup>



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## **Education:**

PhD students David Xu, Brent Trenhaile, Andrew Signor, and Aba Agrawal, undergraduate Philip Waggoner, and research associate Koji Nakayama contribute to this program. David Xu was recognized with a best student poster; he will receive either the AVS Varian or Hoffman Award in November 2003.



A pantomime of the roughening reaction

## **Outreach:**

Six freshmen are involved in a project that focuses on surface patterning. They will present their work during Engineering Open House, an event that draws 30,000 visitors, young and old, to campus each year.



entranced EOH audience